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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/655,595	09/06/2000	William F. Beausoleil	POU9-2000-0045-US1	9321

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ORRICK, HERRINGTON & SUTCLIFFE, LLP
4 PARK PLAZA
SUITE 1600
IRVINE, CA 92614-2558

EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 05/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/655,595	BEAUSOLEIL ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1/31/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5 were examined.

Section I Response to Applicants Remarks

Drawings

2. Applicants are thanked for addressing this issue. Objection is withdrawn.

Specification

3. Applicants are thanked for addressing this issue. Examiner acknowledges amended IDS. Objection is withdrawn.

Design Choice

3b. Examiner acknowledges applicant's response while stating the design choice explanation wasn't intended as a rejection.

35 U.S.C. § 112 Second Paragraph

4. Applicants are thanked for addressing this issue. The rejections are withdrawn.

35 U.S.C. § 103(a)

5. Applicant's arguments are persuasive; therefore rejection is withdrawn. However another ground of rejection has been considered by Catlin (U.S. Patent 4,797,604 (1989)) in view of Nishikdawa (U.S. Patent 6,122,443 (2000)).

Section II: Rejection (4th Office Action)

Specification

6. The amendment filed 1/31/05 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material that is not supported by the original disclosure is as follows:

- *Selected emulation board connector pins on the emulation board(s) comprising the emulation engine are connected through signal interfacing circuits and connectors on a one-for-one basis to the signal pins of the target system. Thus, each input or output signal of the target system is connected to a specified emulation processor output or input signal. Similarly, emulation processors may be connected to the monitoring and data capturing facilities.*

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 103

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being obvious by Catlin (U.S. Patent 4,797,604 (1989)) in view of Nishikdawa (U.S. Patent 6,122,443 (2000)).

Catlin teaches an in-circuit emulation of a processor that is mounted on a circuit board (abstract); but doesn't teach determining wire length. Nishikdawa teaches a method of wire length minimization (abstract).

At the time of invention, it would have been obvious to one of ordinary skill in the art to modify Catlin by way of Nishikdawa to effectively minimize the total wire length while avoiding an excess change to the layout (Nishikdawa: column 6, lines 15-20).

Claim 1. In an emulator that includes printed circuit boards (Catlin column 1, lines 15-24; column 1,lines 48-50) interconnected by a multi-conductor cable (Catlin: column 1, lines 29-32) with inputs at one end of the cable and corresponding outputs at the other cable end, a method for determining the length of the cable (Nishikdawa: column 6, lines 1-35) while the cable is installed in the emulator thereby interconnecting the printed circuit board comprising: prior to installing the cable, interchanging the inputs or

outputs of at least one pair of conductors (Catlin: column 2, lines 43-48) of the multi-conductor cable to denote a cable length (Nishikdawa: column 6, lines 1-35); inputting a test pattern to the cable (Catlin: column 3, lines 25-33) said test pattern comprised of binary data; collecting an output data pattern from the cable that results from the test pattern (Catlin: column 3, lines 45-50); determining the cable length (Nishikdawa: column 6, lines 1-35) from the output pattern (Catlin: column 3, lines 45-50); compiling an emulation program to account for each interchanged pair of conductors, the emulation program corresponding to a logical design for an integrated circuit (Catlin: column 3, lines 19-33).

Claim 2 The method for determining the length of the cable as in claim 1 (Catlin column 1, lines 15-24; column 1,lines 48-50; Nishikdawa: column 6, lines 1-35) wherein said test pattern is a pattern of alternating (inherent: logic devices or microprocessors, Catlin: column 1, lines 8-10) binary "1" and "0s."

Claim 3. The method for determining the length of the cable as in claim 1(Catlin column 1, lines 15-24; column 1,lines 48-50; Nishikdawa: column 6, lines 1-35) wherein one cable length is denoted by having no interchanged pair of conductors (defined output signals, thus defined inputs, Catlin: column 2, lines 52-56) .

Claim 4. The method for determining the length of the cable as in

claim 2 wherein one cable length is denoted by having no interchanged pair of conductors (Catlin: column 3, lines 19-33).

Claim 5. A method for determining length of a multi-conductor cable installed in an emulation system, the emulation system having a first printed circuit board electrically communicating with a second printed circuit board (Catlin column 1, lines 15-24; column 1,lines 48-50) via the multi-conductor cable so that the emulation system (Catlin: column 1, lines 29-32) can execute an emulation program corresponding to a logic design, the multi-conductor cable having a plurality of inputs at one end and a corresponding plurality of outputs at the other end, comprising: prior to installing the cable, interchanging the inputs or outputs of at least one pair of conductors (Catlin: column 3, lines 45-50) of the multi-conductor cable to denote a cable length (Nishikdawa: column 6, lines 1-35); inputting a test pattern to the cables said test pattern comprised of binary data (inherent: logic devices or microprocessors, Catlin: column 1, lines 8-10); collecting an output data pattern from the cable that results from the test pattern; determining the cable length from the output pattern (Nishikdawa: column 6, lines 1-35); compiling the emulation program ("diagnostic feature", Catlin: column 1, lines 35-39) so that the interchanged pair of conductors is accounted for when the emulation program is run on the emulation system.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tom Stevens whose telephone number is (703) 305-0365, Monday-Friday (8:30 am- 5:30 pm) or contact Supervisor Mr. Kevin Teska at (703) 305-9704. The fax number for the group is 703-872-9306.

Any inquires of general nature or relating to the status of this application should be directed to the Group receptionist whose phone number is (703) 305-3900.

May 9, 2005

THS

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER